Технологии Интел для высокопроизводительных вычислений

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8 июля **2010**

Летняя школа «Суперкомпьютерное моделирование и визуализация в научных исследованиях»

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Программа

- Почему высокопроизводительные вычисления важны для Intel
- Основные технологические проблемы
- Следующие шаги в HPC с Intel

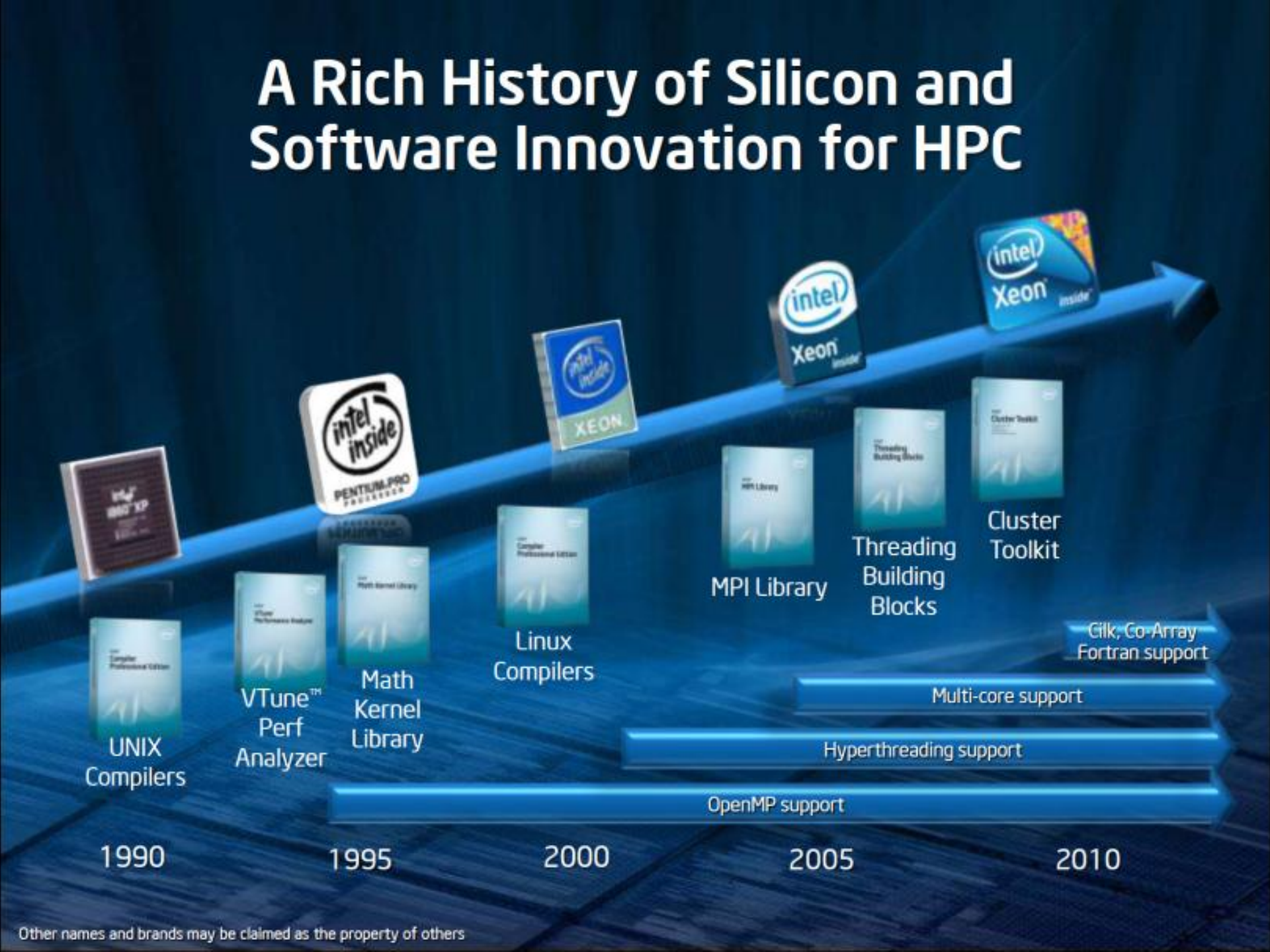
25 Years Also = Intel Beginnings in HPC: "The Cosmic Cube"

Intel iPSC/1

- Scalable from 32 to 128 nodes
  - Intel 80286 microprocessor
  - Intel 80287 math coprocessor
  - 512K RAM local memory
  - Ethernet-connected hypercube
- Peak performance of 3.2 MFLOPS

Cosmic Cube image © Marvel Comics

A Rich History of Silicon and Software Innovation for HPC



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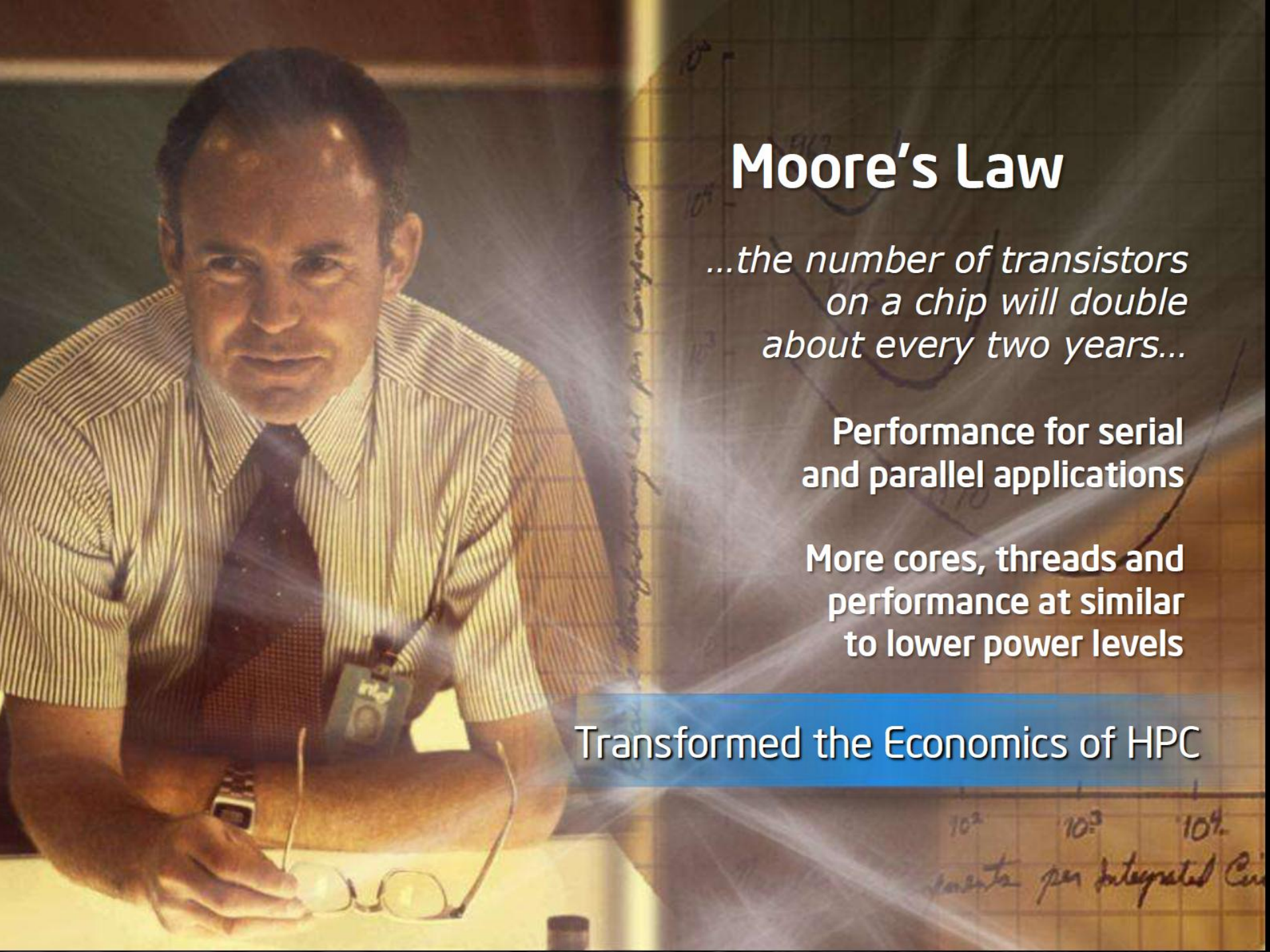
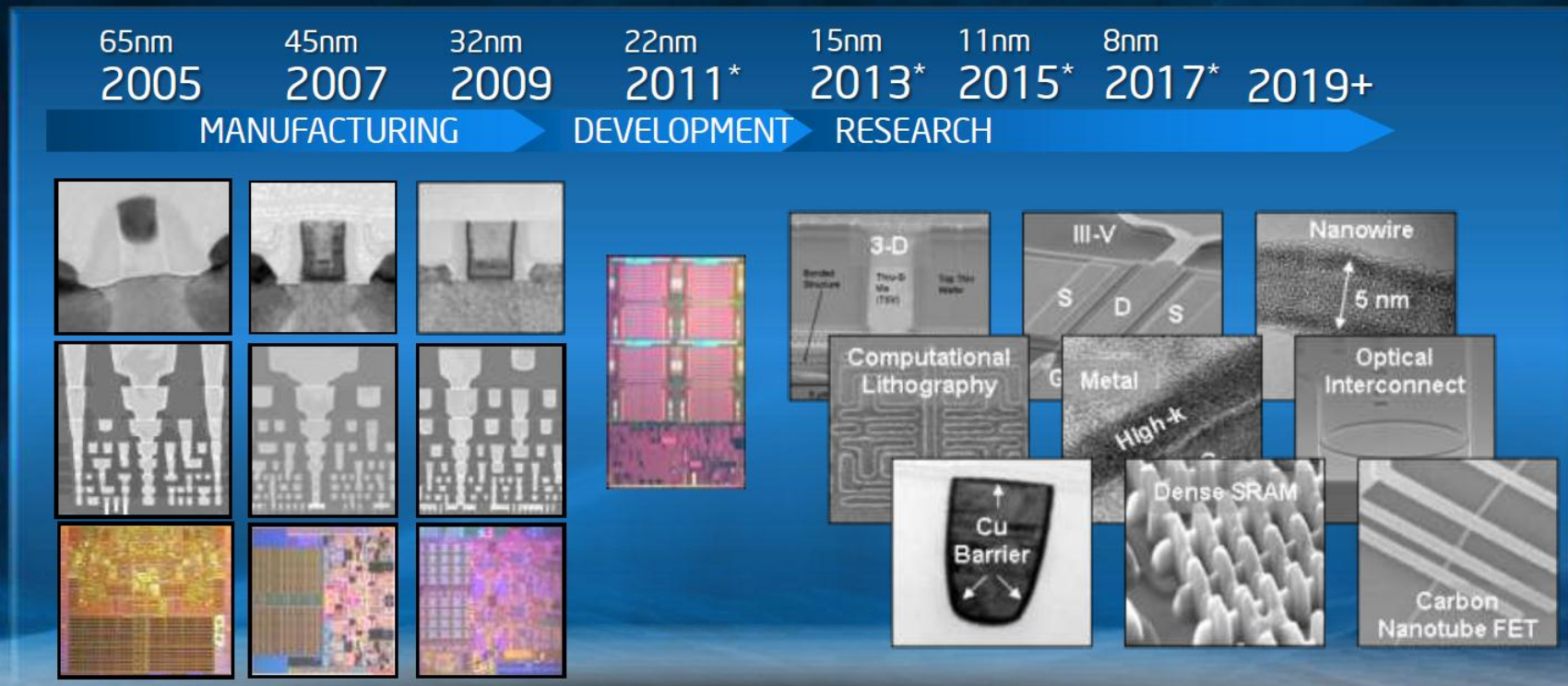

Moore's Law
...the number of transistors on a chip will double about every two years...
Performance for serial and parallel applications
More cores, threads and performance at similar to lower power levels
Transformed the Economics of HPC

Moore's Law: Alive and Well at Intel



Intel Innovation-Enabled Technology Pipeline is Full

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High Performance Micro-Architecture for PetaScale Deployments

intel Xeon inside™

intel

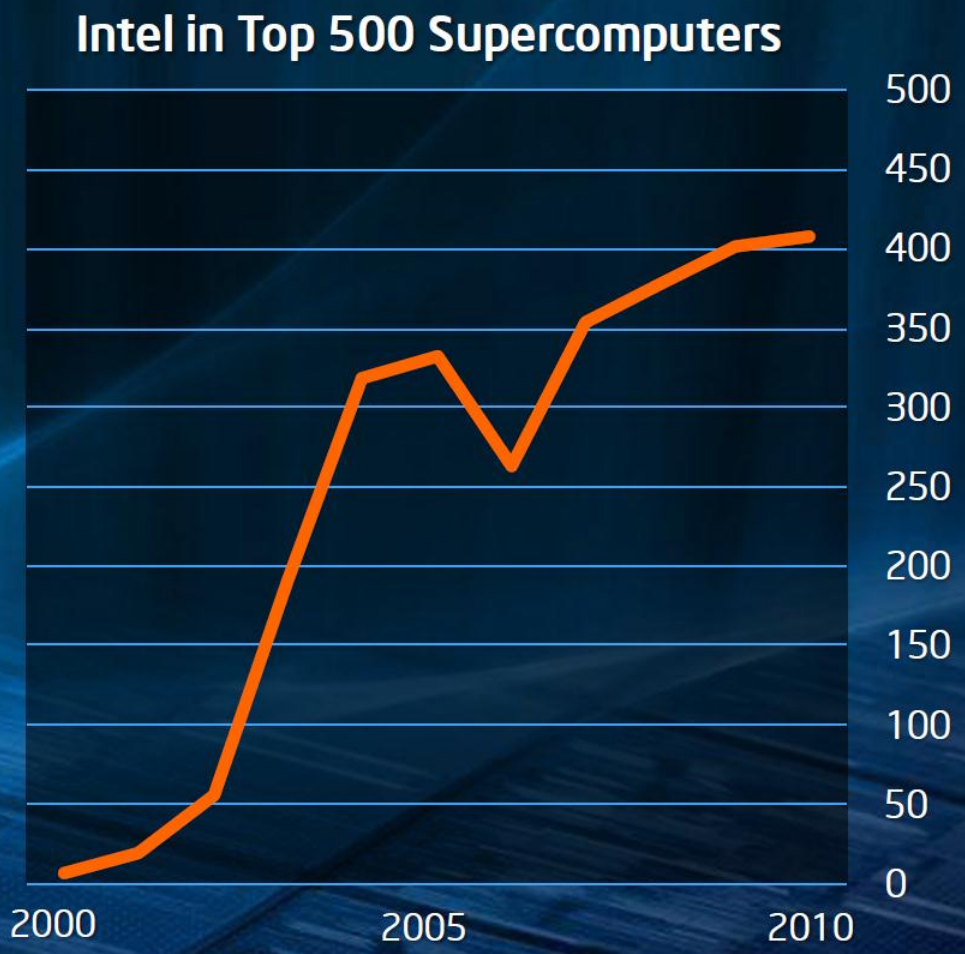
Intel Top 500 Market Adoption

Value Proposition:

Volume economics

IA programming model

Robust ecosystem



Source: www.top500.org

Почему высокопроизводительные вычисления важны для Intel

- Intel in 408 of 500 systems*
  - NEW Intel® Xeon® processor 5600 series in 7 systems
  - NEW Intel® Xeon® processor 7500 series in 2 systems
  - Intel® Xeon® processor 5500 series in 184 systems
  - ~93% of the new listings are IA based
- Powering the Top Systems
  - 4 newest listings in top 10 are powered by Intel Architecture; 2 with Intel Xeon processor 5600 series
  - 6 of 7 new Top 30 systems are Intel Architecture

*All data sources from Top 500.org, June 2010

Top 500 June 2010: Causes for Concern?

As expressed in the Top500 update:

- Lowest average performance increase
- Drop in number of new listings
- No new technology shift underway (by core count)
- Has Moore's Law stopped delivering?

Does this signal a challenge getting to ExaScale?

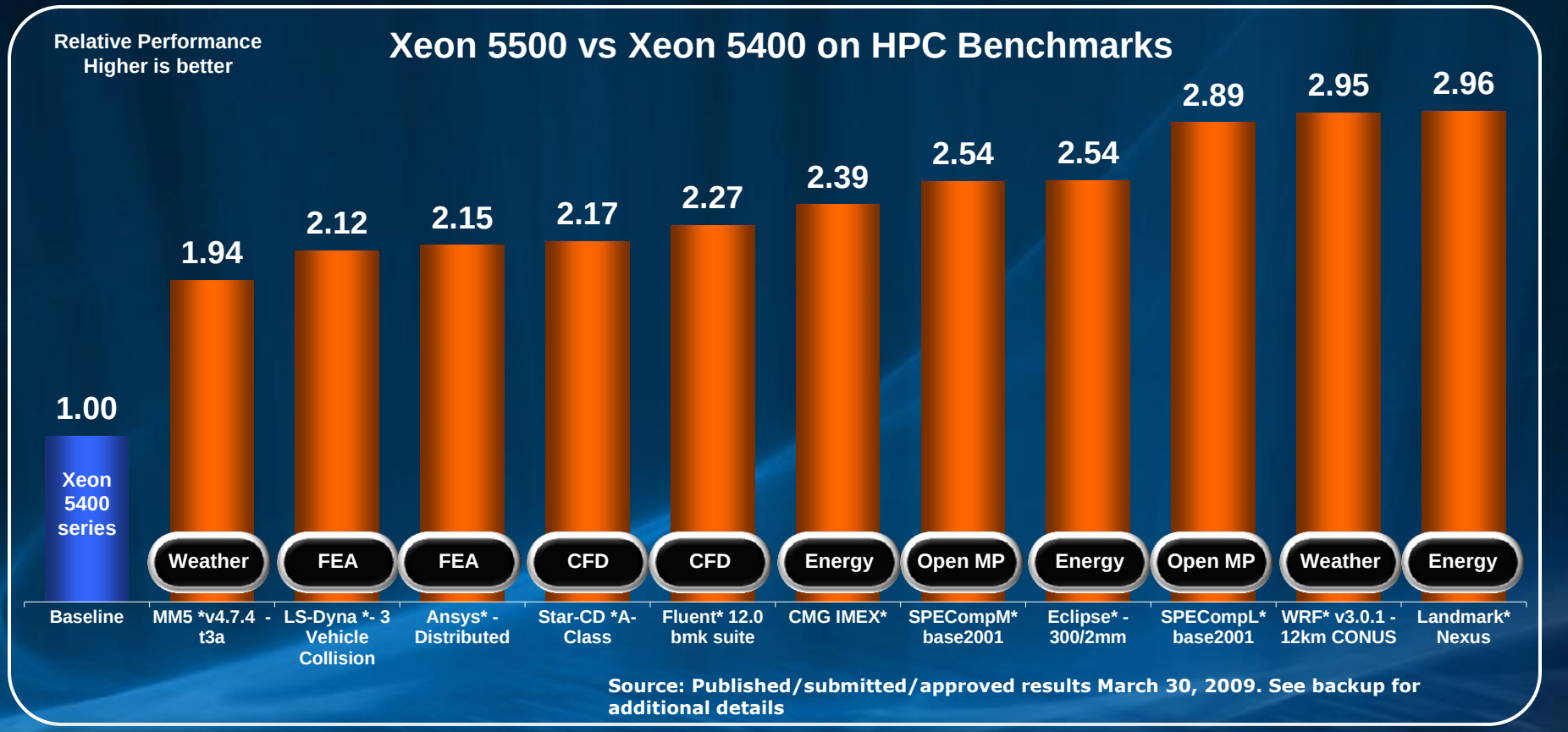
Assertion: the answer to all of the above is No

No new technology transition?

- Core count trends show next transition going slowly
- However, the latest technology shift IS underway:
- The Intel Xeon processor architecture formerly codenamed 'Nehalem' has gone from
  - June 2009: 33 7%
  - Nov 2009: 95 19%
  - June 2010: 193 39%
- That's a pretty rapid technology shift…
- With what impact?

All data sources from Top 500.org

Intel® Xeon Processor 5500 Comparison



*Up to 2-3X performance improvement on many applications. But only modest gains on Linpack**

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Performance efficiency also counts…

Summary of systems with high speed interconnect

Average Top 500 system Linpack efficiency	
Pure Nehalem architecture based (IB)	88%
Systems with GPGPUs (IB)	42%
All other systems (no GbE)	78%

Which would you rather have?

All data sources from Top 500.org

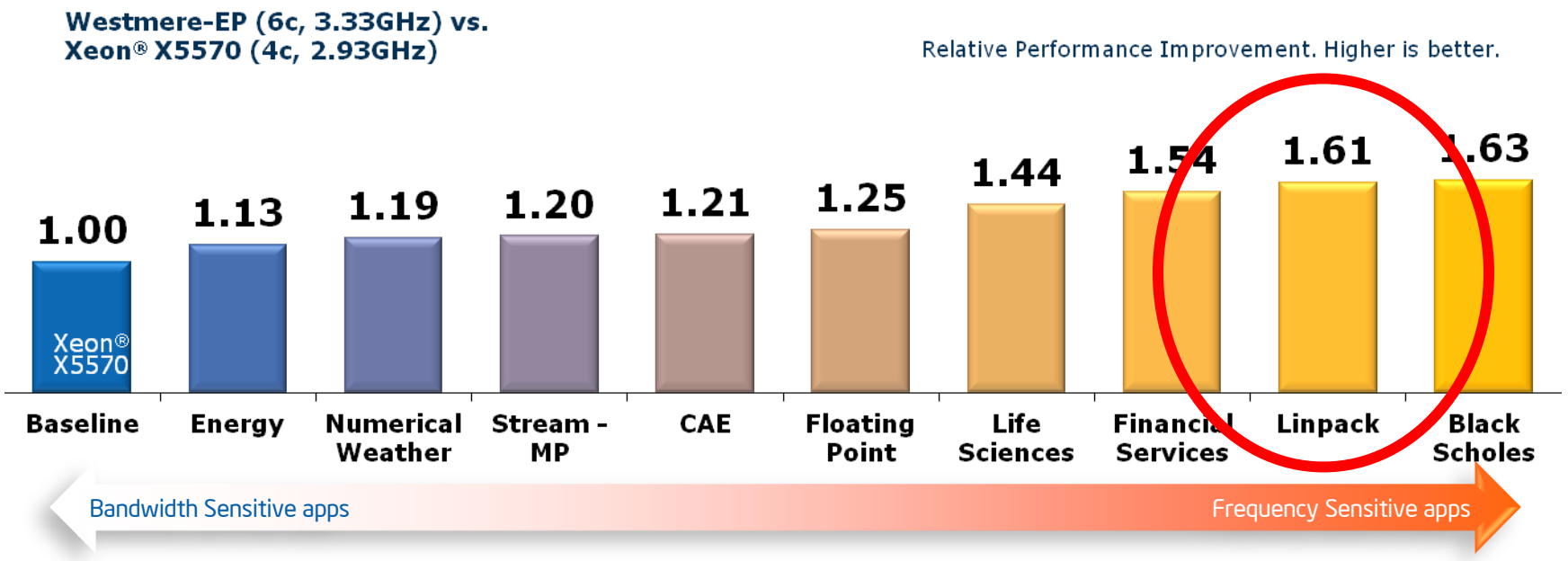
So what ?

- Nehalem showed modest improvement on Linpack*
  - But many applications saw up to 2-3X performance
  - …and this microarchitecture already nearly 40% of the list
- So, the new Top 500 systems HAVE delivered a big performance improvement, just not on Linpack
- …and Nehalem architecture delivers high efficiency
- Corollaries:
  - Core count is not the best or only indicator
  - Not all cores are created equal
  - Top 500 continues rapid adoption of new technology

Will this change? Yes!

Intel® Xeon® processor 5600 – the new generation of intelligent performance

HPC Applications, SPECfp*_rate & STREAM



>60% improvement projected for Linpack

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The Next Generation Xeon Processor
Sandy Bridge "Tock"

- Significantly greater performance with higher core-count & Intel® Hyper-threading Technology
- 2x Flops / clock peak using new AVX instructions

Making Petascale Widely Available for Leading Science

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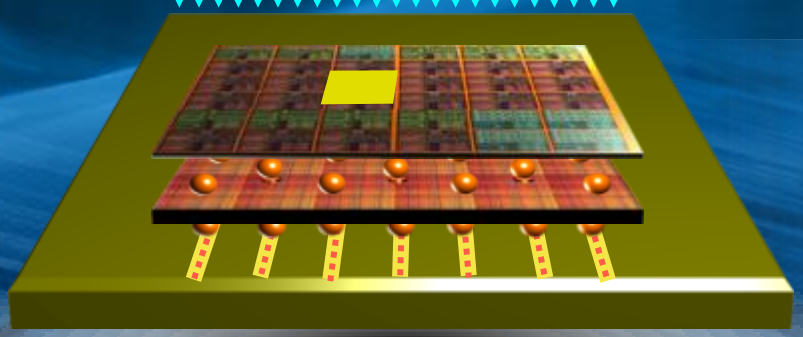
PetaScale Programming Challenges

Irregular Patterns and Data Structures

?

Scale to Multi-Core → Hard
Scale to Many-Core→ Harder



Increasing number of cores & threads
Vector instructions

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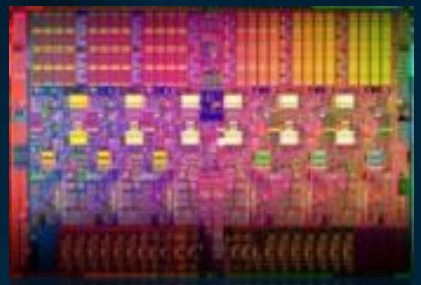
IA Programming Flexibility



intel® Software

Instruction Parallelism	Data Parallelism	Thread Parallelism	Cluster / Process Parallelism

Serial Code Node Level
Fast Scalar performance, Optimized C/C++,FORTRAN, Threading and Performance Libraries, Debug / Analysis Tools

Parallel Node Level
Multi-core, Multi-Socket, SSE and AVX instructions, OpenMP, Threading Building Blocks, Performance Libraries, Thread Checker , Ct , Cilk

Multi-Node / Cluster Level
Cluster Tools, MPI Checker

Programming choices and standards for range of parallel efficiency

intel

Simplifying Software Development:
Intel® Software Development Tools

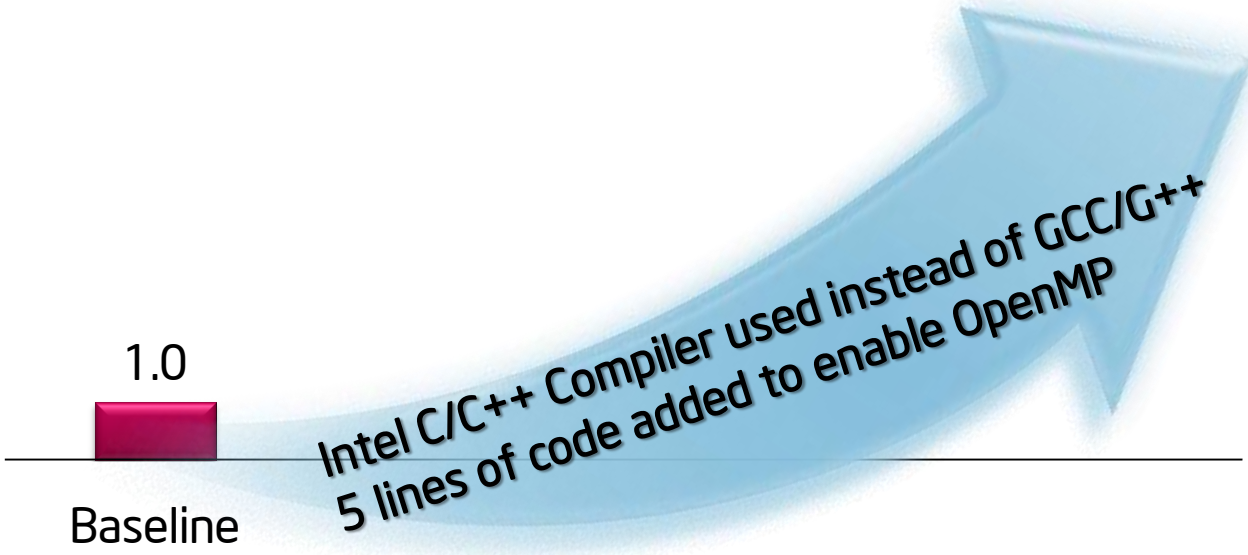
Parallel Studio	HPC Tools	Cluster Tools
Essential Parallelism	Advanced Parallelism	Distributed Parallelism

Tools to preserve your source code investments

Taking advantage of Intel Tools and Standard Programming Model

Intel® Xeon® processor 5600 Performance

ClustalW - Multiple Sequence Alignment



Over 8x improvement after 20 minutes of work

Leveraging 12 cores on Xeon X5670 Processor-based server

The copyright for ClustalW and ClustalX is held by Des Higgins, Julie Thompson and Toby Gibson. ClustalW version used is 2.0.12.
Source: Intel internal measurements. See backup for the details.
Notes: Performance is obtained on specific customer model with 430 sequences. Performance improvement may vary with other input datasets.

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Parallel Programming Education

2K universities in 88 countries

4K faculty trained

320K students trained

intel.com/thinkparallel

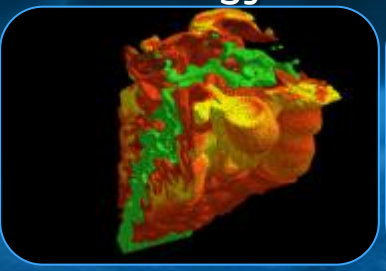
Source: Evans Data Corporation, Intel

Exascale: *The Next Frontier*

Challenges

- Power – energy / operation of computation, data transport, memory
- Threading software to millions/billions of threads
- Memory/Storage capacity and bandwidth
- Managing high-node count systems in the existence of failures (MTBF)
- Affordability

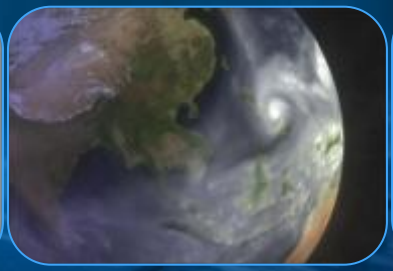
Energy



Physics

Biology

Climate



Astrophysics

Intel committed to solving the challenges of Exascale

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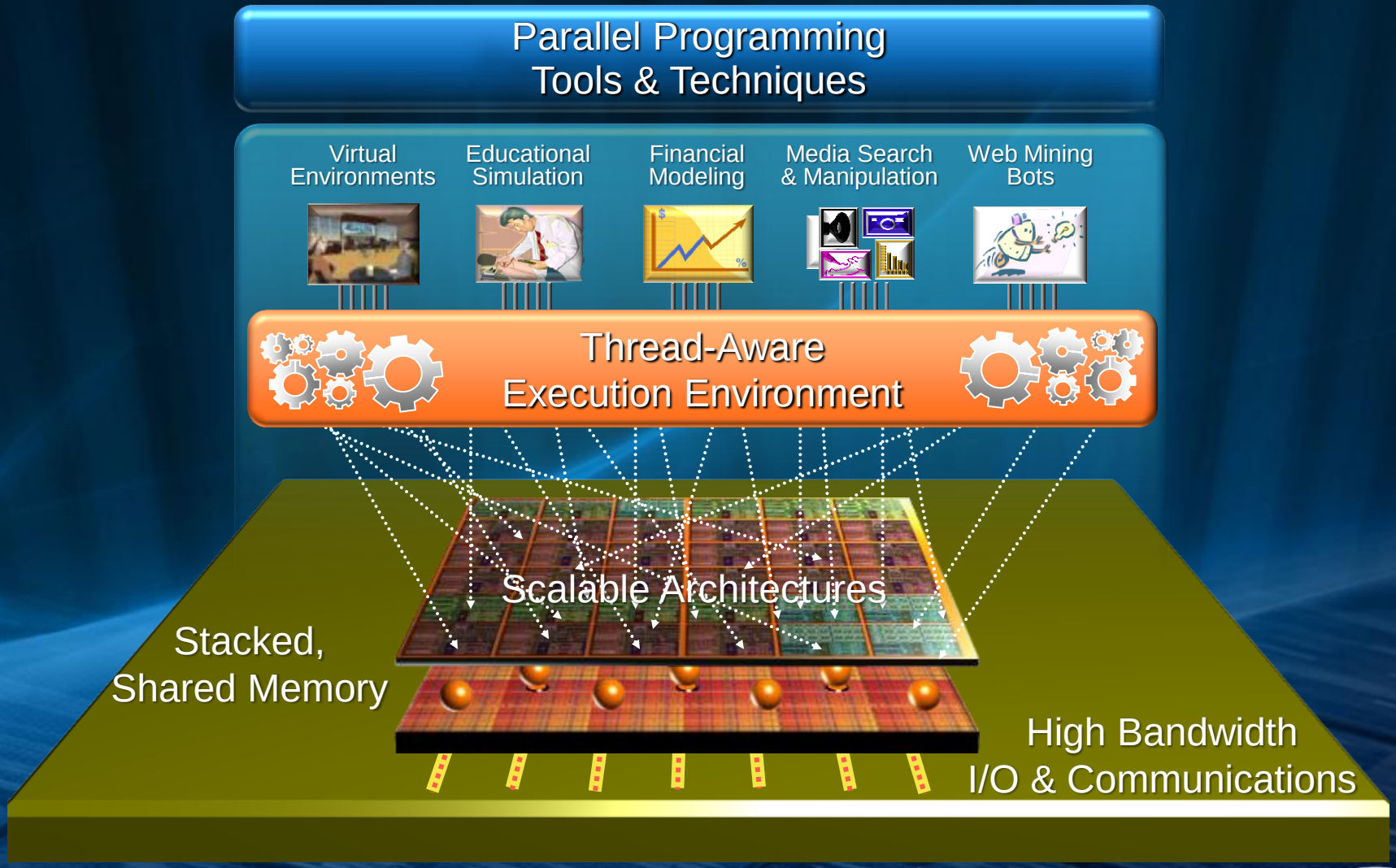
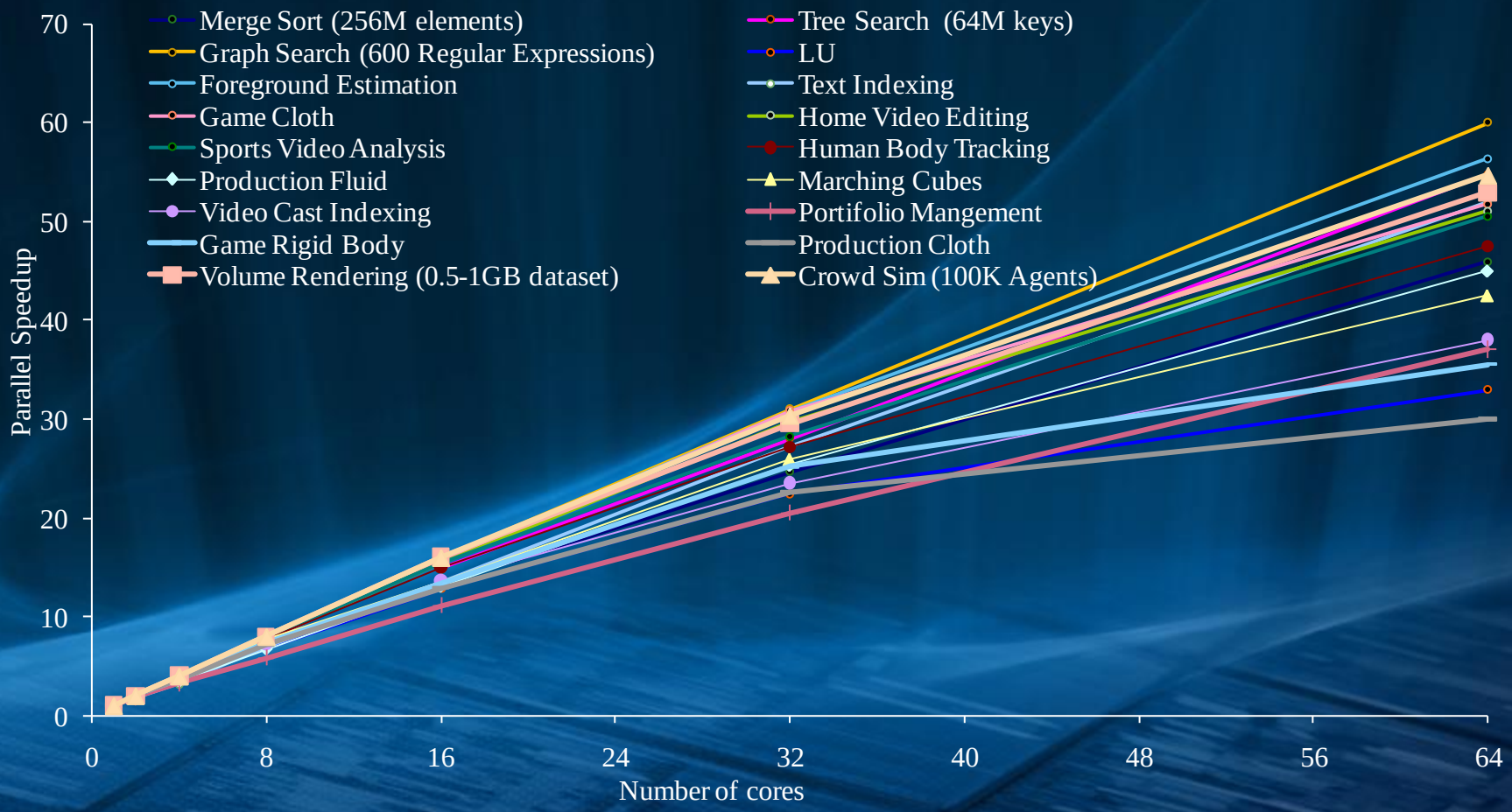
Intel's Many-Core Research Program



Application-Driven Architecture Research

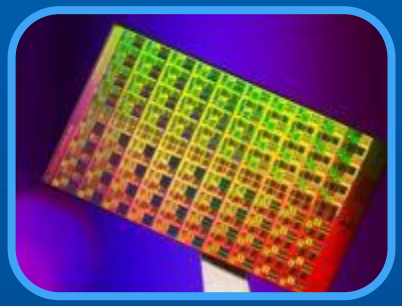


Constantly Evaluating Options for All Workloads

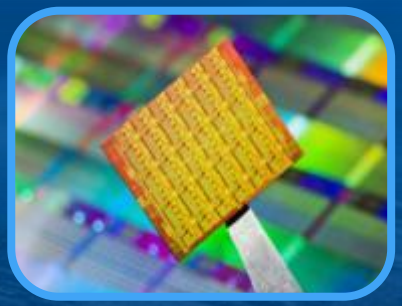
Source: Intel

Intel Labs
Parallel Computing Research

Research Processors from Intel Labs



Tera-scale Research Processor
Mar 2007



Single Chip Cloud Computer
Dec 2009

Architecture with Many Cores

Demonstrated Intel McRT ("Manycore Runtime") 11 Issue 03

Carbon: Architectural Support for Fine-Grained Parallelism on Chip Multiprocessors

Physical Simulation for Animation and Visual Effects: Parallelization and Characterization for Chip Multiprocessors

Scaling performance of interior-point method on large-scale chip multiprocessor system

2008

Second Life and the New Generation of Virtual Worlds

Larrabee: A Many-Core x86 Architecture for Visual Computing

Atomic Vector Operations on Chip Multiprocessors

Efficient Implementation of Sorting on Multi-Core SIMD CPU Arch

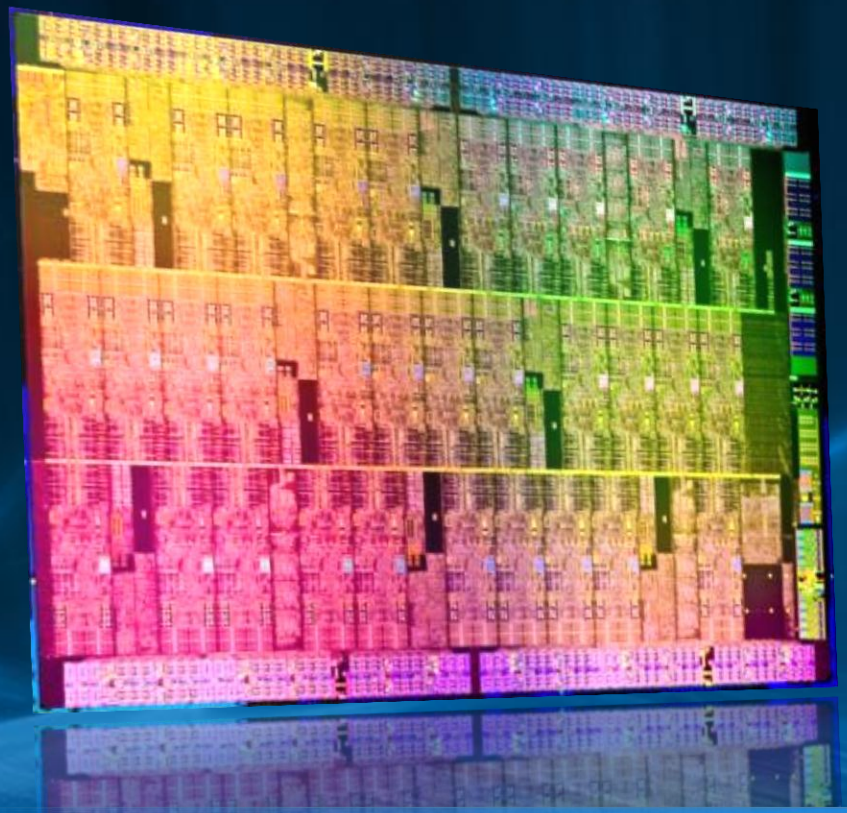
Convergence of Recognition, Mining, and Synthesis Workloads and Its Implications

Accelerating Video-Mining Applications Using Many Small, General-Purpose Cores

2009

Mapping High-Fidelity Volume Rendering for Medical Imaging to CPU, GPU and Many-Core Architectures

From Research to Realization.
Announced last week at ISC Hamburg:



Intel®
Many
Integrated
Core
Architecture

The Newest Addition to the Intel Server Family.
Industry's First General Purpose Many Core Architecture

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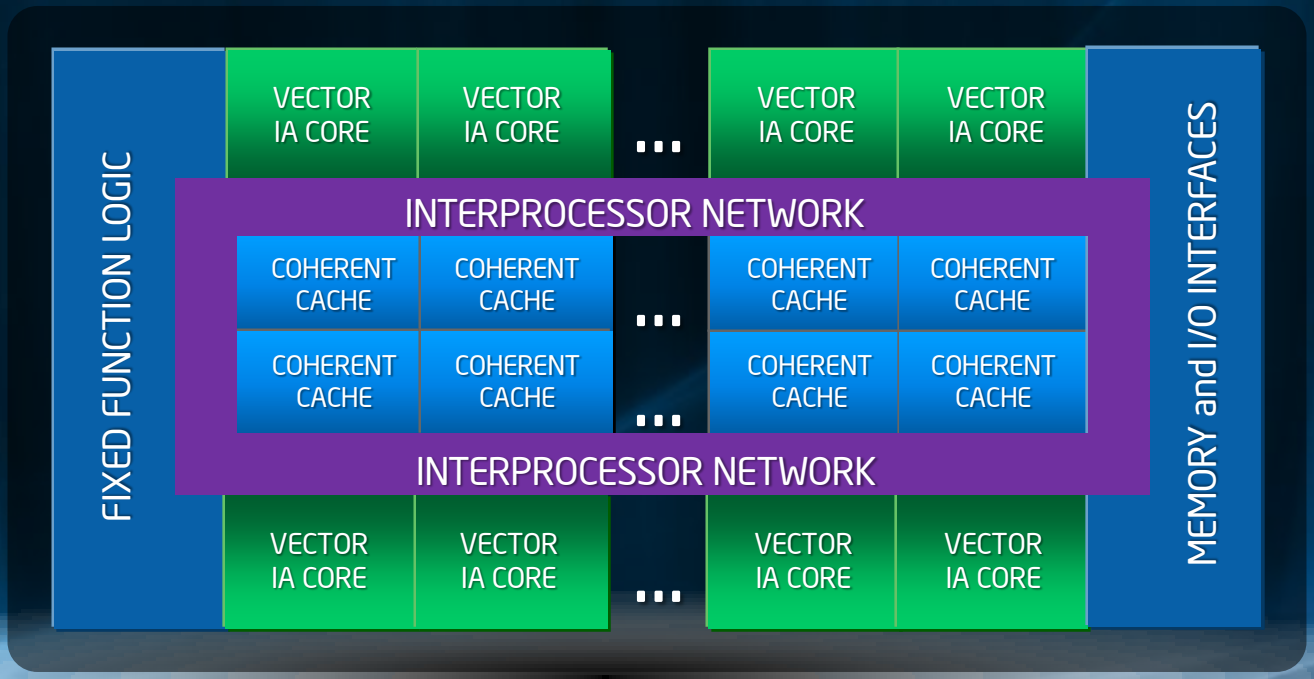
Intel® MIC Architecture:
An Intel Co-Processor Architecture



Many cores and many, many more threads

Standard IA programming and memory model

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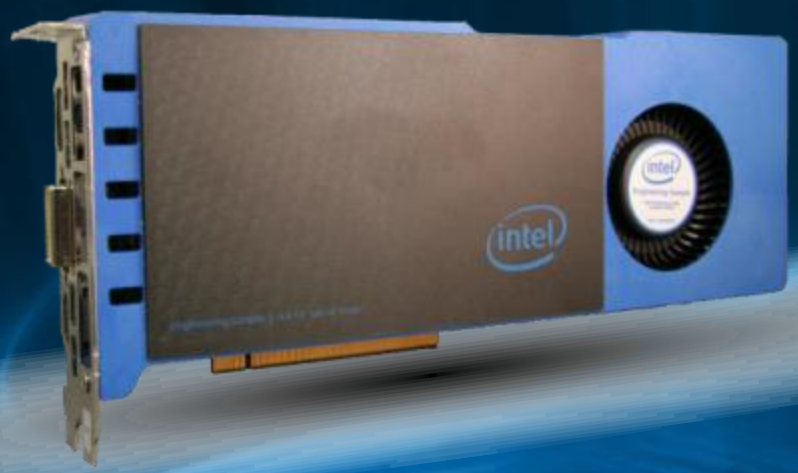
Knights Ferry



- Software development platform
- Growing availability through 2010
- 32 cores, 1.2 GHz
- 128 threads at 4 threads / core
- 8MB shared coherent cache
- 1-2GB GDDR5
- Bundled with Intel HPC tools

Software development platform for Intel® MIC architecture

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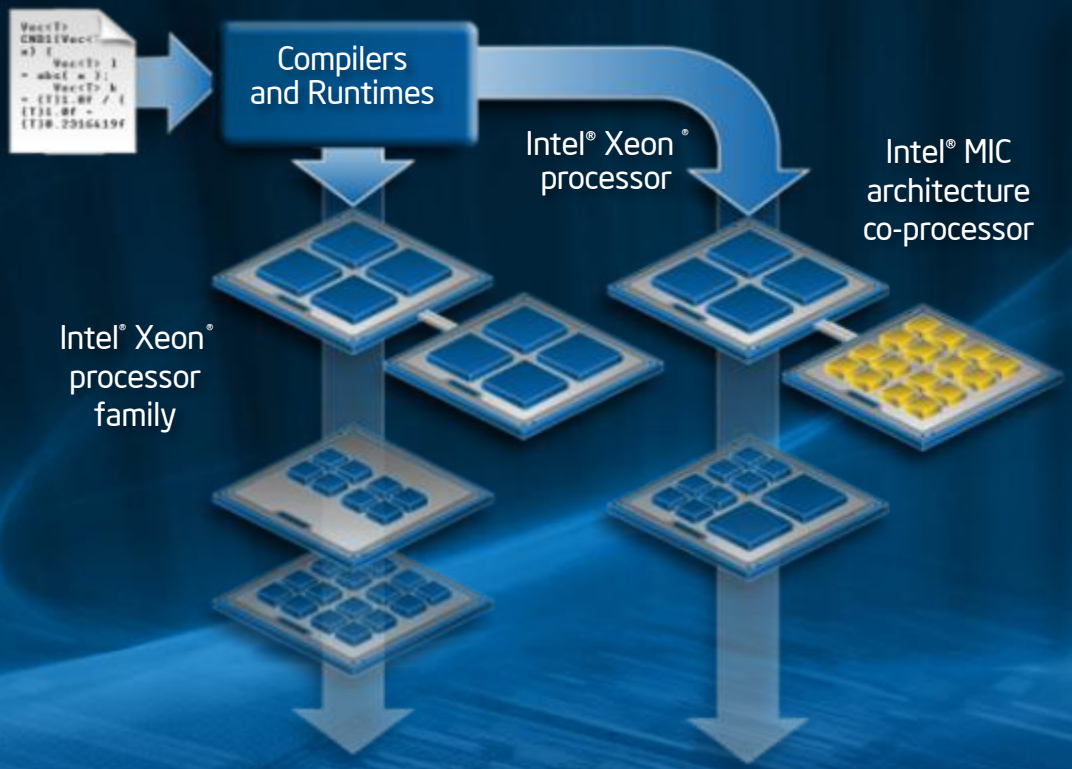
Intel® MIC Architecture Programming

Single Source



Common with Intel® Xeon®

- Languages
- C, C++, Fortran compilers
- Intel developer tools and libraries
- Coding and optimization techniques
- Ecosystem support

Eliminates Need for Dual Programming Architecture

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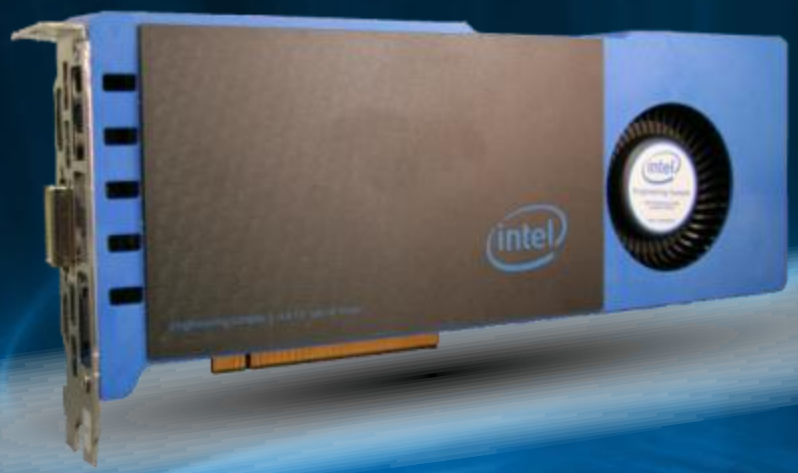
Knights Ferry Demonstration @ISC 2010



Demo team challenge:

Showcase LU benchmark with minimal tuning – “you have 3 days…”

Best previously published 3rd party result found** is 380 GFLOPS

Leading LU result demonstrated on 5/31/10*: >500GF !

* Single Knights Ferry @1.2GHz with 1GB GDDR5

** Towards Dense Linear Algebra for Hybrid GPU Accelerated Manycore Systems; Stanimire Tomov, Jack Dongarra and Marc Baboulin: January 2009; (RBT LU algorithm single precision)

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Семейство со-процессоров Knights

Knights Products

Knights Corner

1st Intel® MIC product

22nm process

>50 Intel Architecture cores

Knights Ferry

intel

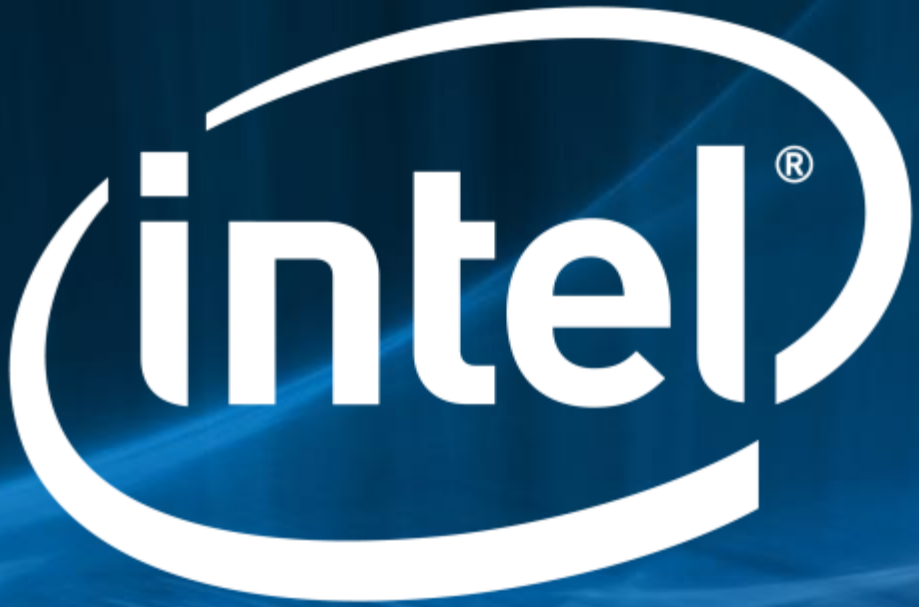
Выводы

- Технологии Intel использовались в ~93% новых суперкомпьютерах в списке Top500
- Эффективность важна: не все ядра одинаково эффективны
- Программное обеспечение и алгоритмы это самое дорогое что есть у наших клиентов

Новые направления инвестиций Intel в HPC:

- Новое: Архитектура Intel® Many Integrated Core (MIC)
- Новое: Инструменты разработки для гетерогенных систем
- Новое: Семейство со-процессоров Knights
  - Knights Ferry – платформа для разработки и оптимизаци ПО
  - Knights Corner – продукт на базе 22nm и >50 ядер IA

Thank you!



Sponsors of tomorrow

Intel® Xeon 5500 series processors

System Configuration Information

All comparisons based on published/submitted/approved results as of March 30, 2009

Fluent: Comparison based on published/submitted results to www.fluent.com/software/fluent/fl6bench/fl6bench_6.4.x/index.htm as of March 30, 2009. All comparisons were using results run on 8 cores within a single machine on dual socket quad-core servers.

- Baseline Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+* server platform with two Intel® Xeon® processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux 5.3*. Performance measured using Fluent Version 12.0 Beta. (Version 12.0.13)*. Six individual benchmarks are shown as a measure of single node performance. "Overall" performance is the geometric mean of the six individual benchmarks.
- Intel® Xeon® processor X5570 based platform details: SGI Altix ICE 8200EX* server platform with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI 6.4 MT/sec, 24GB memory (12x2GB 1066MHz DDR3), 64-bit Suse Linux Enterprise Server* 10 SP2 with ProPack 6SP2*. Performance measured using Fluent Version 12.0 Beta. (Version 12.0.9) Six individual benchmarks are shown as a measure of single node performance. "Overall" performance is the geometric mean of the six individual benchmarks.
- Quad-Core AMD Opteron* processor model 2384 platform based details:Server platform with two AMD Opteron 2384 processor 2.7GHz, 6MB L3 cache, Linux OS. Performance measured using Fluent Version 12.0 Beta. (Version 12.0.7) Six individual benchmarks are shown as a measure of single node performance. "Overall" performance is the geometric mean of the six individual benchmarks.

SPECompM2001

- Baseline Intel® Xeon® processor E5472 based platform details: Supermicro X7DB8+ server platform* with two Intel Xeon processors E5472 3.0GHz, 12MB L2 cache, 1600MHz FSB, 32GB memory (8x4GB 800MHz DDR2 FB-DIMM), SUSE LINUX 10.1* (X86-64) (Linux 2.6.16.13-4-smp). Binaries built with Intel Compiler 10.1. Referenced as published at 17187. (SPECompMbase2001). For more information see http://www.spec.org/omp/results/res2007q4/omp2001-20071107-00274.html.
- Intel® Xeon® processor X5570 based platform details: Cisco B-200 M1 server platform* with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, 6.4GT/s QPI, 24 GB memory (6x4 GB DDR3-1333MHz), Red Hat EL 5.3, Linux Kernel 2.6.18-128.el5 SMP x86_64, Binaries built with Intel® C/C++ Compiler 11.0 for Linux. Result submitted to www.spec.org for review at 43593 (SPECompMbase2001) as of March 30, 2009.
- Quad-Core AMD Opteron processor 2384 based platform* details: Supermicro H8DMU Server platform* with two Quad-Core AMD Opteron processors 2386SE* 2.80GHz, 6MB L3 cache, 16GB memory (8x2GB, PC2-6400, Reg, dual-rank CL5), SUSE Linux Enterprise Server 10 64-bit, Binaries built with PathScale Compiler Suite*, Release 3.1. Referenced as published at 22678 (SPECompMbase2001). For more information http://www.spec.org/omp/results/res2008q4/omp2001-20081021-00320.html.

Multiphysics Finite Element Analysis using ANSYS* - Comparison based on published/submitted results to www.ansys.com/services/hardware-support-db.htm as of March 30, 2009.

- Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+* server platform with two Intel® Xeon® processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux 5.1*. Performance measured using ANSYS* Mechanical* 12.0 Preview 7. Benchmark for Ansys-Shared* consists of a suite of 8 workloads and Ansys-Distributed* consists of a suite of 7 workloads. Geo mean of each these workload groups used for comparison.
- Intel® Xeon® processor X5570 based platform details: Supermicro X8DTN+ server platform with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI 6.4 MT/sec, 24GB memory (12x2GB 1066MHz DDR3), 64-bit RedHat Enterprise Linux 5.3. Performance measured using ANSYS* Mechanical* 12.0 Preview 7. Benchmark for Ansys-Shared consists of a suite of 8 workloads and Ansys-Distributed consists of a suite of 7 workloads. Geo mean of each these workload groups used for comparison.

MM5 v4.7.4 - t3a and **WRF v3.0.1 - 12km CONUS** : Comparison based on measured results as of March 30, 2009. All comparisons were using results run on 8 cores within a single machine on dual socket quad-core servers. Same platform used for both benchmarks

- Baseline Intel® Xeon® processor X5482 based platform details: SGI Altix ICE 8200EX* server platform with two Intel® Xeon® processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit Suse Linux Enterprise Server* 10 SP2 with ProPack 6SP2*.
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Intel® Xeon 5500 series Processors

System Configuration Information

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Reservoir Simulation using Schlumberger Eclipse*

- Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+ server platform* with two Intel Xeon processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux 5.3*. (64-bit) and Eclipse version 2008.1 software.
- Intel® Xeon® processor X5570 based platform details: Supermicro X8DTN+ server platform* with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI 6.4* MT/sec, 24GB (12x2GB 1066MHz DDR3) memory, 64-bit RedHat Enterprise Linux 5.3. Eclipse version 2008.1 software.

Reservoir Simulation using Landmark Nexus*

- Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+ server platform* with two Intel Xeon processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux 5.2*. (64-bit) . Landmark Nexus R5000 software*.
- Intel® Xeon® processor X5560 based platform details: Supermicro X8DTN+ server platform* with two Intel Xeon processors X5560 2.80GHz, 8MB L3 cache, QPI 6.4 MT/sec, 12GB memory, 64-bit RedHat Enterprise Linux 5.3. Landmark Nexus R5000 software.
- **Reservoir Simulation using CMG* IMEX***
- Intel® Xeon® processor X5482 based platform details: Dell Precision T7400 platform* with two Intel Xeon processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 32GB RedHat Enterprise Linux 5.2*. (64-bit) CMG IMEX, Version 2008.11.
- Intel® Xeon® processor X5570 based platform details: Supermicro X8DTN+ server platform* with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI 6.4* MT/sec, 18GB memory. RedHat Enterprise Linux 5.3. (64-bit) CMG IMEX, Version 2008.11.

Computational Fluid Dynamics analysis using Star-CD* (Single Node) - Comparison based on published/submitted results to http://www.cd-adapco.com/products/STAR-CD/performance/406/index.html as of March 30, 2009. All comparisons were using results run on 8 cores within a single machine on dual socket quad-core servers.

- Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+* server platform with two Intel Xeon processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux 5.3*. Performance measured using STAR-CD v4.06. Same configuration used for all both benchmark results - A-Class and C-Class.
- Intel® Xeon® processor X5570 based platform details: Supermicro X8DTN+* server platform with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI* 6.4 MT/sec, 24GB memory (12x2GB 1066MHz DDR3), 64-bit RedHat Enterprise Linux 5.3. Performance measured using STAR-CD v4.06. Same configuration used for all both benchmark results - A-Class and C-Class.

Crash Simulation analysis using LS-DYNA* (Single Node): Comparison based on published/submitted results to http://www.topcrunch.org/ as of March 30, 2009. All comparisons were using results run on 8 cores within a single machine on dual socket quad-core servers.

- Intel® Xeon® processor X5482 based platform details: Supermicro X7DB8+* server platform with two Intel® Xeon® processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 16GB memory (8x2GB 800MHz DDR2 FB-DIMM), 64-bit RedHat Enterprise Linux* 5.3. Performance measured using LS-DYNA mpp971.s.R321. Same configuration used for all three benchmark results - neon_refined_revised, 3 vehicle collision, car2car.
- Intel® Xeon® processor X5570 based platform details: Supermicro X8DTN+ server platform with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, QPI 6.4 MT/sec, 24GB memory (12x2GB 1066MHz DDR3), 64-bit RedHat Enterprise Linux 5.3. Performance measured using LS-DYNA mpp971.s.R321. Same configuration used for all three benchmark results - neon_refined_revised, 3 vehicle collision, car2car.

SPECompL2001

- Baseline Intel® Xeon® processor E5472 based platform details: Supermicro X7DB8+ server platform* with two Intel Xeon processors X5482 3.20GHz, 12MB L2 cache, 1600MHz FSB, 32GB memory (8x4GB 800MHz DDR2 FB-DIMM), SUSE LINUX 10.1* (X86-64) Intel Compiler 11.0. Submitted to www.spec.org for review at 81332 as of March 30, 2009.
- Intel® Xeon® processor X5570 based platform details: Cisco B-200 M1 server platform* with two Intel Xeon processors X5570 2.93GHz, 8MB L3 cache, 6.4GT/s QPI, 24 GB memory (6x4 GB DDR3-1333MHz), Red Hat EL 5.3, Linux Kernel 2.6.18-128.el5 SMP x86_64, Binaries built with Intel® C/C++ Compiler 11.0 for Linux. Result submitted to www.spec.org for review at 234,996 (SPECompMbase2001) as of March 30, 2009.

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System Configurations
for Computational Chemistry, bio-informatics, and ClustalW benchmarks

	Xeon X5570 Platform	Xeon X5670 Platform	Xeon X5680 Platform
Platform	Supermicro 2U server SDP	Intel Urbana 1U server SDP	Supermicro 2U server SDP
Processor	Intel Xeon X5570 (Nehalem-EP), 2.93GHz	Intel Xeon X5670 (Westmere-EP), 2.93GHz, B1	Intel Xeon X5680 (Westmere-EP), 3.33GHz, B1
Number of cores	4 per socket	6 per socket	6 per socket
Last Level Cache	8MB	12MB	12MB
Un-core Frequency	2.4GHz	2.4GHz	2.66GHz
QPI Link Speed	6.4GT/s	6.4GT/s	6.4GT/s
Memory	24 GB, DDR3-1333, 6x4GB	24 GB, DDR3-1333, 6x4GB	24 GB, DDR3-1333, 6x4GB
BIOS version	Rev 04/19/2010	Rev 04/19/2010	Rev 04/19/2010
BIOS Settings • Hyper Threading • HW Prefetch • ACL Prefetch • Turbo mode • NUMA mode	 = enabled = enabled = enabled = enabled = enabled	 = enabled = enabled = enabled = enabled = enabled	 = enabled = enabled = enabled = enabled = enabled
OS Distribution	Red Hat EL5-U5, kernel 2.6.18-194.el5	Red Hat EL5-U5, kernel 2.6.18-194.el5	Red Hat EL5-U5, kernel 2.6.18-194.el5

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